关于测试覆盖率

- 随着半导体工艺的发展，可测性技术(DFT)成为每个芯片在设计中必须考虑的问题
- 测试覆盖率作为DFT技术中的关键指标，受到多种因素制约
- 本文针对测试覆盖率的产生算法和结果做一个分析和总结
- 实际案例的具体分析和计算
- 希望对大家的面试和工作有帮助

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What is DFT ?

- DFT strategies that :
  - Improve quality by detecting defects
  - Make it easier to generate vectors
  - Reduce vector generation time
  - Reduce cost

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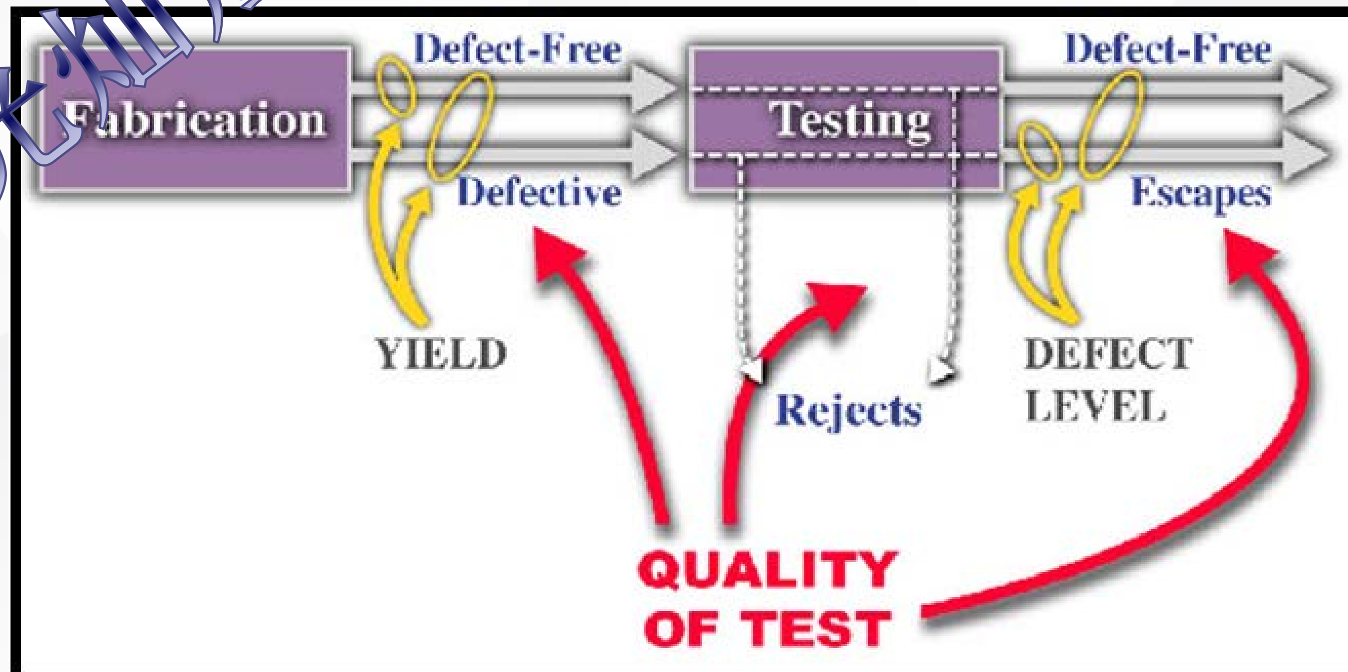

Why Design-for-Test?

- To increase Productivity:
  - Shorter time-to-market
  - Reduced design cycle
  - Reduced cost
- To improve Quality:
  - Reduced Defects per million (DPM)
  - Improved quality of test

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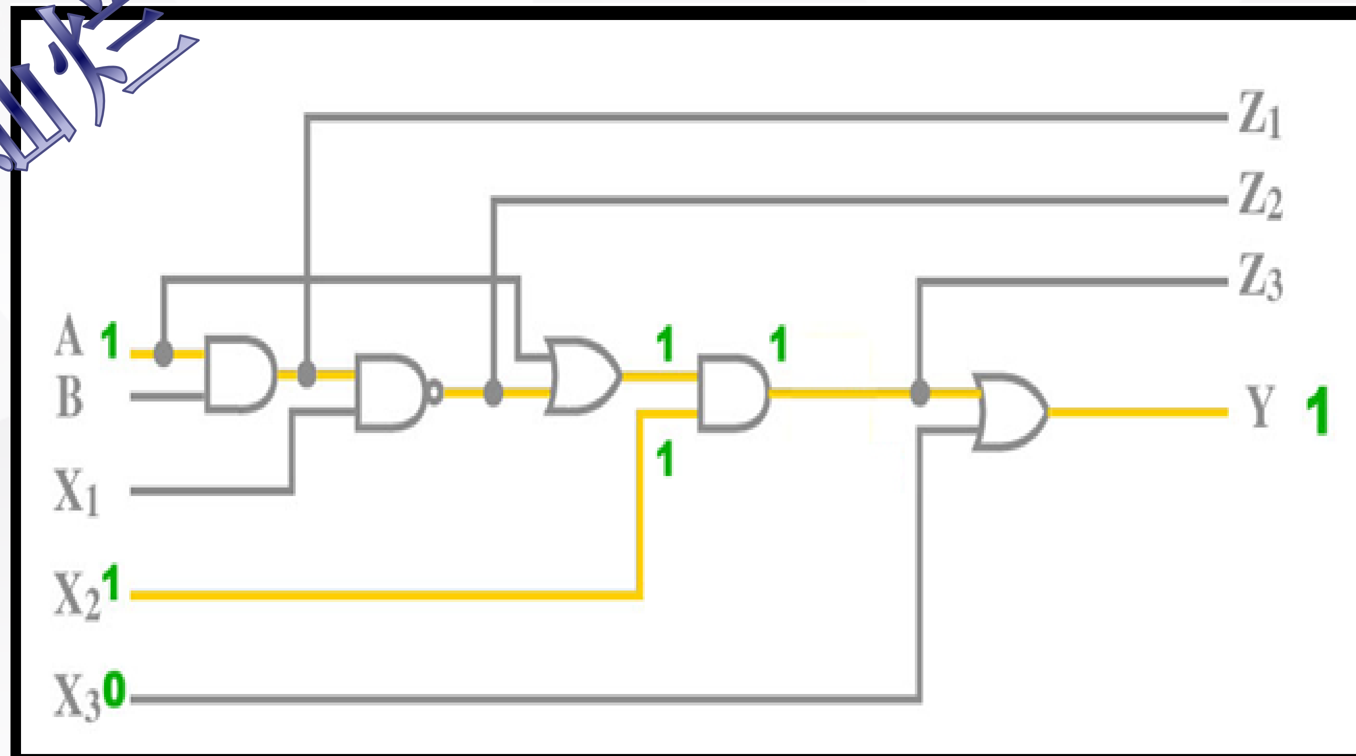
What is Testability?

- Controllability:
  - The ability to set a node to a specific value
- Observability:
  - The ability to observe a node’ s value



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Fault Models

- Fault models:
  - Stuck-at-fault
  - Transition fault
  - Path delay
  - IDDQ

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- Testable fault classes
  - Detected (DT)
    - det_simulation (DS)
      - faults detected when the tool performs fault simulation
    - det_implication (DI)
      - faults detected when the tool performs learning analysis
    - The list are only for path delay testing
      - det_robust (DR)
        - robust detected faults
      - det_functional (DF)
        - functionally detected faults

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- Testable fault classes
  - Posdet (PD):
    - It includes all faults that fault simulation identifies as possible-detected but not hard detected
    - The posdet class contains two groups:
      - posdet_testable (PT) - potentially detectable posdet faults. A higher abort limit may reduce the number of these faults
      - posdet_untestable (PU) - proven AU during pattern generation and hard undetectable posdet faults
    - By default, the calculations give 50% credit for posdet faults

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- Testable fault classes
  - ATPG_untestable (AU)
    - It includes all faults for which the test generator is unable to find a pattern to create a test, and yet cannot prove the fault redundant
    - You cannot detect them by increasing the test generator abort limit

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- Testable fault classes
  - Undetected (UD)
    - It includes undetected faults that cannot be proven untestable or ATPG_untestable
    - The undetected class contains groups:
      - uncontrolled (UC) - undetected faults, which during pattern simulation, never achieve the value at the point of the fault required for fault detection—that is, they are uncontrollable
      - unobserved (UO) - faults whose effects do not propagate to an observable point
    - a higher abort limit may reduce the number of UC or UO faults

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- Untestable fault classes
  - untestable faults (UT)
    - Unused (UU)
    - Tied (TI)
    - Blocked (BL)
    - Redundant (RE)

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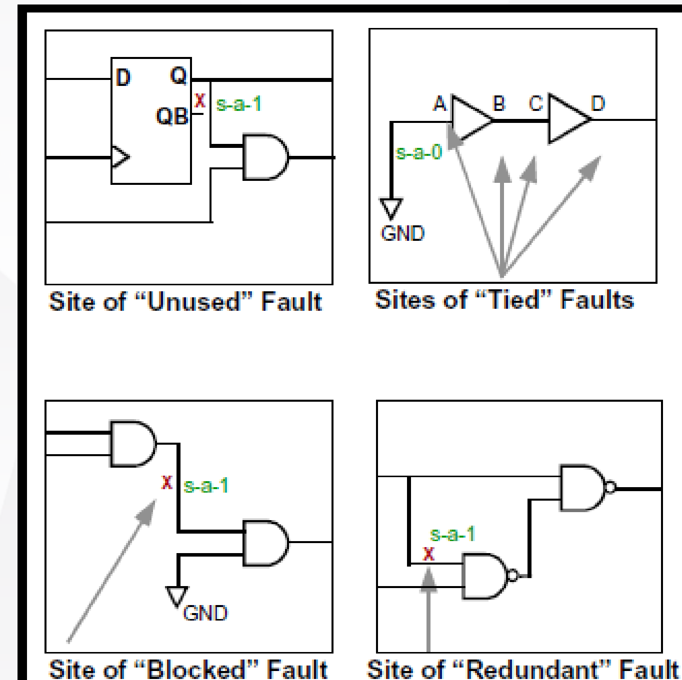

Site of “Unused” Fault
Sites of “Tied” Faults
Site of “Blocked” Fault
Site of “Redundant” Fault

Testability Calculations

Test Coverage

- A measure of test quality, is the percentage of faults detected from among all testable faults
- The tool calculates test coverage using the formula:

$$\frac{\#DT + (\#PD * \text{posdet_credit})}{\#\text{testable}} \times 100$$

- posdet_credit is the user-selectable detection credit (the default is 50%)

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Testability Calculations

- Fault Coverage
  - Fault coverage consists of the percentage of faults detected from among all faults that the test pattern set tests—treating untestable faults the same as undetected faults
  - The tool calculates fault coverage using the formula:

$$\frac{\#DT+(\#PD* \text{posdet_credit})}{\#full} \times 100$$

  - posdet_credit is the user-selectable detection credit (the default is 50%)

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Testability Calculations

- ATPG Effectiveness
  - It measures the ATPG tool's ability to either create a test for a fault, or prove that a test cannot be created for the fault under the restrictions placed on the tool
  - The tool calculates ATPG effectiveness using the formula:

$$\frac{\#DT+\#UT+\#AU+\#PU+(\#PT * posdet_credit)}{\#full} \times 100$$

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实例

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Stuck-at Faults

Fault Classes	#faults (total)	#faults (total relevant)
FU(full)	16816	16782
UO (unobserved)	67 (0.40%)	same (0.40%)
DS (det_simulation)	13598 (80.86%)	same (81.12%)
DI (det_implication)	1565 (9.31%)	same (9.34%)
PU (posdet_untestable)	8 (0.05%)	same (0.05%)
PT (posdet_testable)	22 (0.13%)	same (0.13%)
UU (unused)	90 (0.54%)	same (0.54%)
TI (tied)	9 (0.05%)	same (0.05%)
RE (redundant)	1397 (8.31%)	same (8.33%)
AU (atpg_untestable)	60 (0.36%)	6 (0.04%)
Fault Sub-Classes		
AU (atpg_untestable)		
EDT (edt_blocks)	54 (0.32%)	deleted
PC (pin_constraints)	1 (0.01%)	same (0.01%)
Unclassified	5 (0.03%)	same (0.03%)
Coverage		
test_coverage	99.07%	99.42%
fault_coverage	90.26%	90.55%
atpg_effectiveness	99.54%	99.54%

■实例

■计算过程

- ■FU=UO+DS+DI+PU+PT+UU+TI+RE+AU
- ■PD=PT+PU
- ■test_cov= ((DS+DI+0.5*PD)/(FU-UU-TI-RE))*100=99.42%
- ■fault_cov=((DS+DI+0.5*PD)/FU) *100=90.55%
- ■atpg_eff=((DS+DI+UU+TI+RE+AU+PU+PT*0.5)/FU)*100=99.54%

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